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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,493	01/30/2001	David W. Duemler	D6570-00003	1363

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EXAMINER	
NGUYEN, LE V	
ART UNIT	**PAPER NUMBER**
2174	6

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/772,493	DUEMLER, DAVID W.
	Examiner	Art Unit
	Le Nguyen	2174

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment A, filed 1/30/04.

2. Claims 1-22 are pending in this application; and, claims 1, 9, 17 and 20 are independent claims. This action is made Final.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. Claims 1, 9, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 5,917,483) and Pasquali (US 6,535,882).

Claims 1, 9, 17, and 20:

Duncan et al. (US 5,917,483) teaches a method, apparatus, computer readable medium, and computer data signal for programming a programmable logic controller (col. 3, lines 30 – 40). All software requires a method, apparatus, computer readable medium, and computer data signal for programming a programmable logic controller. Duncan teaches a programmable logic controller including a plurality of inputs and a plurality of outputs (col. 3, lines 30 – 40). Duncan teaches a programmable logic controller directing a process through output signals at said outputs in response to input signals at said inputs (col. 3, lines 30 – 40). Duncan teaches displaying a user on a monitor a graphical data entry user interface (UI) for a plurality of sequential steps, said graphical data entry a user interface representing respective inputs to be monitored by said programmable logic controller at each of said sequential steps and respective

outputs to be initiated by said programmable logic controller at respective ones of said sequential steps (col. 3, lines 30 – 40). Duncan fails to teach monitoring sequential steps and identifying at least one output selected by said user to be initiated for said at least one of said sequential steps.

Pasquali (US 6,535,882) teaches receiving via said graphical data entry user interface, an identification of at least one input selected by said user to be monitored for at least one of said sequential steps and an identification of at least one output selected by said user to be initiated for said at least one of said sequential steps (col. 12, lines 1 – 25). Pasquali teaches converting said identification of said at least one input selected by said user into an input control data table, said input control data table including a plurality of input control data elements (col. 12, lines 1 – 25). Pasquali teaches input control data element corresponding to a respective one of said plurality of sequential steps (col. 12, lines 1 – 25). Pasquali teaches a respective one of said input control data elements representing said at least one input selected by said user (col. 12, lines 1 – 25). Pasquali teaches converting said identification of said at least one output selected by said user into an output data table (col. 11, lines 39 – 56). Pasquali teaches a plurality of output data elements each of said output data elements corresponding to a respective one of said plurality of sequential steps, a respective one of said output data elements representing said at least one output selected by said user (col. 11, lines 39 – 56).

It would have been obvious to one with ordinary skill in the art at the time of the invention to combine monitoring sequential steps and identifying at least one output selected by said user to be initiated for said at least one of said sequential steps taught by Pasquali with the logic control system disclosed by Duncan. Doing so enables step-by-step processing of the said logic control system.

5. Claims 2 – 5, 8, 10 – 13, 16, 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 5,917,483) and Pasquali (US 6,535,882) as applied to claims 1, 9, 17, and 20 above, and further in view of Paraghamian et al (US 4,358,275).

Claims 2, 10, 18, and 21:

Duncan and Pasquali fail to teach a graphical data entry user interface including a timer enabling command option for each of said plurality of sequential steps and a timer value option for each said plurality of sequential steps. Paraghamian et al (US 4,358,275) teaches graphical data entry user interface including a timer enabling command option for each of said plurality of sequential steps and a timer value option for each said plurality of sequential steps (col. 5, lines 35 – 67). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine a user interface for graphical data entries that include a timer enabling command option for each of said plurality of sequential steps and a timer value option for each said plurality of sequential steps taught by Paraghamian with the logic control system disclosed by Duncan and Pasquali. Doing so enables the control of the processing speed.

Claims 3, 11, 19, and 22:

Paraghamian teaches receiving via said graphical data entry user interface, a selection by said user of a timer enabling command for at least one of said plurality of sequential steps (col. 5, lines 35 – 67). Paraghamian teaches receiving via said graphical data entry user interface, a selection by said user for a timer value for said one of said plurality of sequential steps (col. 5, lines 35 – 67). Paraghamian teaches creating a timer value data table including at least one timer value data element, said timer value data element representing said timer value (col. 5, lines 35 –

67). Paraghamian teaches a respective one of said input control data elements representing said the timer enabling command for said one of said sequential steps (col. 5, lines 35 – 67).

Claims 4 and 12:

Paraghamian teaches an input control data element including a plurality of bits, a subset of said plurality of bits representing individual inputs of said programmable logic controller and at least a remaining one of said plurality of bits representing said timer enable command (col. 5, lines 35 – 67).

Claims 5 and 13:

Duncan and Pasquali fails to teach an input control data element including a plurality of bits and a subset of said plurality of bits representing individual inputs of said programmable logic controller. Paraghamian teaches an input control data element that includes a plurality of bits and a subset of said plurality of bits representing individual inputs of said programmable logic controller (col. 5, lines 35 – 67). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine an input control data element including a plurality of bits and a subset of said plurality of bits representing individual inputs of said programmable logic controller taught by Paraghamian with the logic control system disclosed by Duncan and Pasquali. Doing so enable tracking of data being processed.

Claims 8 and 16:

Duncan and Pasquali fails to teach Duncan and Pasquali fails to teach a subset of said plurality of bits representing individual outputs of said programmable logic controller. Paraghamian teaches output data element including a plurality of bits (col. 5, lines 35 – 67). Paraghamian teaches a subset of said plurality of bits representing individual outputs of said

programmable logic controller (col. 5, lines 35 – 67). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine a subset of said plurality of bits representing individual outputs of said programmable logic controller taught by Paraghamian with the logic control system disclosed by Duncan and Pasquali. Doing so enables the creation of output areas for producing program output.

6. Claims 6, 7, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 5,917,483) and Pasquali (US 6,535,882) as applied to claims 1, 9, 17, and 20 above, and further in view of Trask (US 6,249,355).

Claims 6 and 14:

Duncan and Pasquali fail to teach graphical data entry user interface being a check grid. Trask (US 6,249,355) teaches a graphical data entry user interface being a check grid (col. 7, lines 50 – 60). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine the graphical data entry user interface being a check grid taught by Trask with the logic control system disclosed by Duncan and Pasquali. Doing so enables the user to track various registers and bits within the various registers.

Claims 7 and 15:

Duncan and Pasquali fail to teach downloading said input control data table and said output data table to said programmable logic controller. Trask teaches downloading said input control data table and said output data table to said programmable logic controller (col. 7, lines 24 – 36). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine downloading said input control data table and said output data table to said programmable logic controller taught by Trask with the logic control system disclosed by

Duncan and Pasquali. Doing so enables the user to track various registers and bits within the various registers.

Response to Arguments

7. Applicant's arguments filed in Amendment A have been fully considered but they are not persuasive.

Applicant argued the following:

(a) Duncan provides no disclosure relating to programming a PLCs or interface for allowing a user to program a PLC to execute a sequential process.

(b) Pasquali provides nothing with respect to controlling a sequential process with a PLC or otherwise.

The examiner disagrees for the following reasons:

Per (a), claim 1 proceeds to describe the composition of a PLC with the listing of steps in the recitation: "a method of programming a [PLC]...comprising the steps of..." and corresponding passages have been cited for the steps in the office action. If by "a method of programming a [PLC]...comprising the steps of..." Applicant meant to claim embedding or burning (such is the case with firmware) the software code into the chip, Applicant is invited to incorporate the step(s) describing the embedding or burning of the software code to chip in order to make it enabling.

Per (b), in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In*

re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Duncan teaches displaying to a user a graphical data entry user interface (UI) for a plurality of sequential steps, the graphical data entry being a user interface representing respective inputs to be monitored by the programmable logic controller at each of said sequential steps and respective outputs to be initiated by said programmable logic controller at respective ones of said sequential steps (col. 3, lines 30 – 40).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquires

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Lê whose telephone number is **(703) 305-7601**. The examiner can normally be reached on Monday - Friday from 5:30 am to 2:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine Kincaid, can be reached on (703) 308-0640.

The fax numbers for the organization where this application or proceeding is assigned are as follows:

(703) 872-9306 [Official Communication]

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

LVN
Patent Examiner
April 17, 2004

Kristine Kincaid
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TECHNOLOGY CENTER 2100